**International Journal of Communication Networks and Information Security**
2024, 16(4)
ISSN: 2073-607X,2076-0930
https://ijcnis.org/

**Research Article**

# DESIGN OFMAC USING FEED FORWARD NEURAL NETWORKS

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mathematical function to determine neuron activation and

ARTICLE INFO
Received: 18 Jul 2024
Accepted: 24 Aug 2024

ABSTRACT
This research investigates the usage of feed forward neural networks,traditional Indian Vedic multiplier,carry skip adder,parallel in parallel out register and MAC. An Artificial Neural Network (ANN) operates in a parallel information processing structure, comprising processing units. The efficiency of the network is determined by the processing unit. Hence, there is a need to design a processing unit that is both efficient and capable of delivering superior performance. This processing unit encompasses a MAC unit (Multiplication and Accumulation) and an Activation unit. The main focus of high-speed processors is to minimize power consumption and processing times. The
implementation of the design utilizes Verilog, a hardware description language, and the testing phase is carried out using the Modelism simulator.The study performance the 4 bit mac using feed forward network with 4 bit mac using logic gates.
**Keywords –** Artificial neural network ,MAC, Vedic multiplier, carry skip adder and Verilog HDL.

## 1.INTRODUCTION

Neural networks consist of interconnected processing elements, wherein these elements store interconnection strengths and weights. These networks find extensive application in statistical analysis and data modeling, such as image and speech recognition, character recognition, financial prediction, and geological survey. In this neural network framework, inputs are treated as high dimensional and can be either discrete or real-valued functions. Similarly, the output function is also considered a discrete or real vector-valued function. The computational model of an artificial neuron closely mirrors that of natural neurons. In natural neurons, signals are received through synapses on the neuron membrane. Upon reaching a sufficient signal threshold, the neuron activates and transmits the signal through the axon, potentially activating other neurons through their synapses. In the artificial neuron model, inputs (analogous to synapses) are multiplied by weights and then processed through a compute the output. Artificial Neural Networks (ANNs) amalgamate these artificial neurons to process information, employing a distributed representation of stored information. Typically, the neural network model takes input samples and generates corresponding output samples, with the relationship between input and output functions determined by the network.

Artificial Neural Networks (ANNs) can be categorized into feedforward and feedback networks. In a feedforward neural network, data travels unidirectionally, moving from the input layer through one or more hidden layers to the output layer, devoid of any feedback loops. The versatility of feedforward neural networks, in capturing intricate relationships and patterns, is evident in their applications across diverse fields. Noteworthy examples encompass tasks such as image and speech recognition, natural Language Processing and Financial Prediction.
Efficient multiplication involves crucial processes like partial product addition, where the accuracy is reliant on an effective adder within the multiplier. Carry Skip Adder (CSLA) has been introduced as a

high-speed adder, widely employed in data processing processors for arithmetic operations. In comparison to the Ripple Carry Adder (RCA), the CSLA exhibits reduced delay, thereby enhancing the

speed of addition. While there is a slight increase in area, the CSLA ultimately contributes to lower delay, resulting in an overall improvement in the performance of the Multiply-Accumulate (MAC) unit.

## II. ARTIFICIAL NEURAL NETWORK

An Artificial Neural Network operates as a parallel information processing system, comprising multiple processing units. The term "neural network" transitioned to "Artificial Neural Networks" to clarify its distinction from biological neural networks. ANN is associated with a general computing architecture referred to as Multiple Instruction Multiple Data (MIMD) parallel processing architecture, deviating from its biological counterpart.

Figure 1 depicts the structure of a basic neural network comprising three layers: input, hidden, and outputlayers.

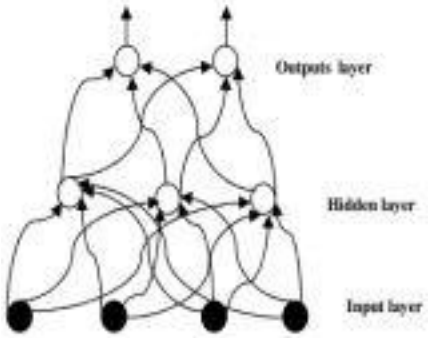


Fig.1.simple neural network

Input data is forwarded to the output through the hidden layer in a simple neural network. Processing between the input and output is facilitated by processing units.In the framework for an Artificial Neural Network (ANN) model, various ANN models exist, and each can be defined by the following elements:A collection of processing units,a state of activation for each unit,an output for each unit and Network topology.An activation rule governing the update of activities for each unit. The external environment serves as the information source for the network. A learning rule is employed to adjust the connectivity structure based on the information from the external environment. Following information processing, the output function utilizes activation values to compute unit outputs. The processing of a MAC (Multiply-Accumulate) unit is illustrated by a simple artificial neuron. MAC operations play a crucial role in ensuring the accuracy of results within neural networks.

Figure 2 illustrates a simple artificial neuron in the artificial neural network, featuring a multiplication and accumulation unit. Each input undergoes individual multiplication with corresponding weights, and the resulting outputs are aggregated using an addition unit. The summed output is then forwarded to an activation unit, which produces an output of 0 or 1 based on a defined threshold.

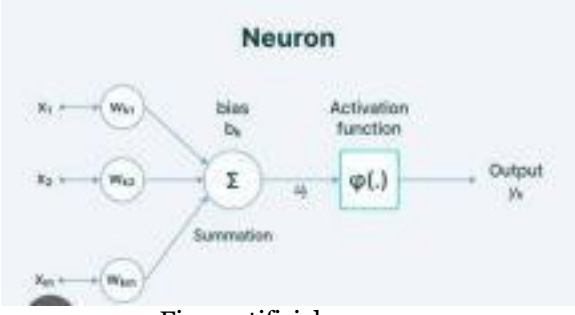


Fig.2.artificial neuron

The most basic form of a feedforward neural network is characterized by a single layer of input nodes fully linked to a layer of output nodes. This network is capable of learning patterns that are linearly separable, employing distinct artificial neurons referred to as threshold logic units (TLU).

Unit step activation function:

The unit step activation function is a frequently employed element in neural networks. It yields an

output of 0 for a negative argument and 1 for a positive argument. The function is defined as follows, with a range between (0, 1), and its output is binary.

III.MAC

The hardware component responsible for executing this function is termed a multiplier-accumulator (MAC or MAC unit). The MAC operation plays a pivotal role in various Digital Signal Processing (DSP) algorithms, particularly in digital filtering. In contemporary computers, there might be a specialized

MAC, comprising a multiplier implemented in combinational logic, succeeded by an adder and an accumulator register to store the outcome. The register's output is looped back to one input of the adder, enabling the addition of the multiplier output to the register on each clock cycle.

The Multiplication and Accumulation (MAC) unit serves as a crucial processing element within the neural network. The accuracy of the network is dependent on the performance of the MAC unit. To execute the MAC operation, a Vedic multiplier with CSL adder was employed.

Multiplier Accumulator (MAC) fig.3 architectures consist of a standard multiplier, adder, and an accumulator module. Within these systems, the newly generated product is combined with the previous MAC outcome through an accumulation adder.

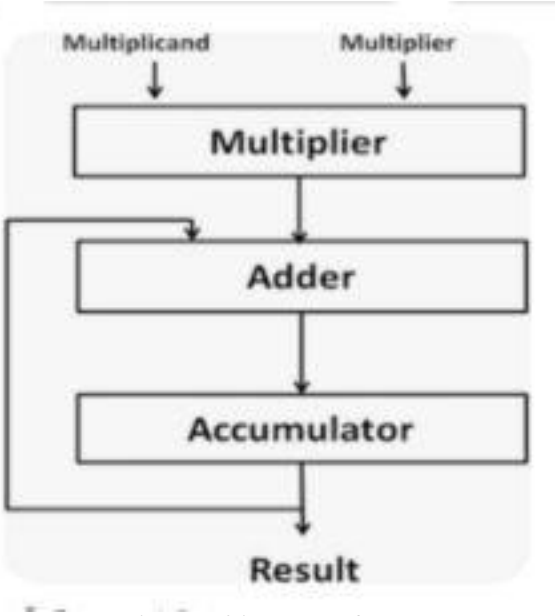


Fig.3.architecture of mac

## IV.VEDIC MULTIPLIER

Multipliers play a vital role in digital circuits and computer architecture, facilitating the multiplication of binary numbers. The design of multipliers encompasses diverse algorithms and architectures, each presenting distinct advantages and trade-offs. In digital circuits, such as those in computers, multipliers are electrical circuits dedicated to multiplying two binary integers. Binary adders were utilized in their construction. Within the

framework of Vedic Mathematics, two distinct approaches, namely vertical and crosswise methods, are employed for rapid multiplication. When compared to

other multipliers, the Vedic multiplier has a shorter delay. The main application of this method is to quickly multiply large numbers.

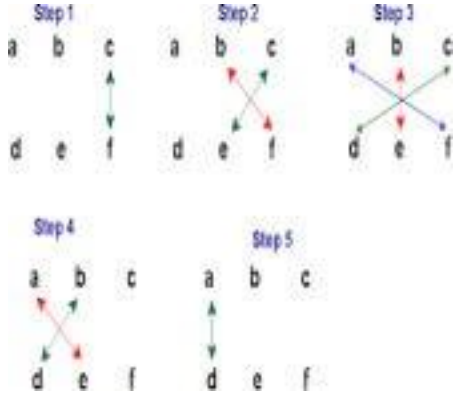

Fig.4.basic multiplication of vedic multiplier

As depicted in Figure 4, consider two three-digit numbers. ancient Vedic method of multiplication employed to obtain the product of these decimal numbers, asshown in the same figure. Using vertical and crosswise multiplication, the technique yields the product of the two numbers.

2*2 vedic multiplier:

In this section, we will be discussing the 2*2 Vedic multiplier. The block diagram for this multiplier can be seen in Figure 1. It utilizes two half adders in its design. Consider thevalues of a being 1:0 and b being 1:0. Fig 2 showcases the output of decimal numbers using Vedic multiplication. Initially, the output is obtaineddirectly from a0b0. The values of a0b1 and a1b0 areprocessed by a half adder, and the resulting

sum is taken as an output. The carry and the value of a1b1 are then passed on to another half adder. In total, theoutput of this is 4 bits binary length.

fig.5.block diagram

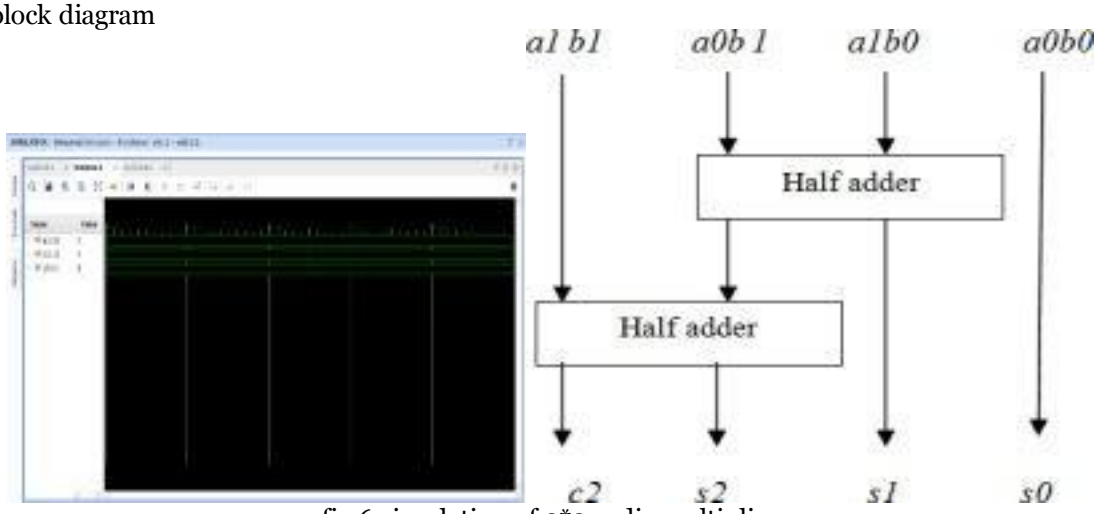


fig.6.simulation of 2*2 vedic multiplier

4*4 Vedic multiplier using Carry skip adder Carry skip adder:

A Carry-Skip Adder, also referred to as a Carry Bypass Adder or a Carry-Lookahead Bypass Adder, is a digital adder circuit employed in digital computing systems to add binary numbers. It falls within the category of adders, alongside Ripple Carry Adders (RCAs) and Carry Lookahead Adders (CLAs). The main objective of a Carry Skip Adder is to minimize the propagation delay linked with carry generation in adder circuits

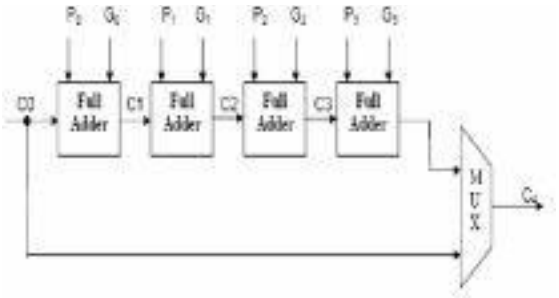


Fig.6 bit carry skip adder

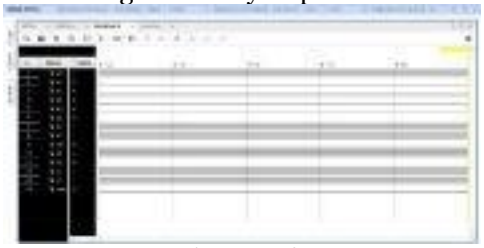

Fig.7.result

4*4 Vedic Multiplier:

This section outlines the functioning of the 4x4 Vedic multiplier, depicted in Figure 2. This employs three 4-bit carry skip adders, four 2-bit Vedic multipliers, and a half adder. The inputs, as illustrated in the diagram, are processed to producethe output, which represents the product of the inputs. the output of 4*4 vedic multiplier is 8 bit binary length.it is given to the 8 bit carry skip adder. A[3:0]

and B[3:0].
A= a3 a2 a1 a0 (multiplicand) B= b3 b2 b1 b0 (multiplier)

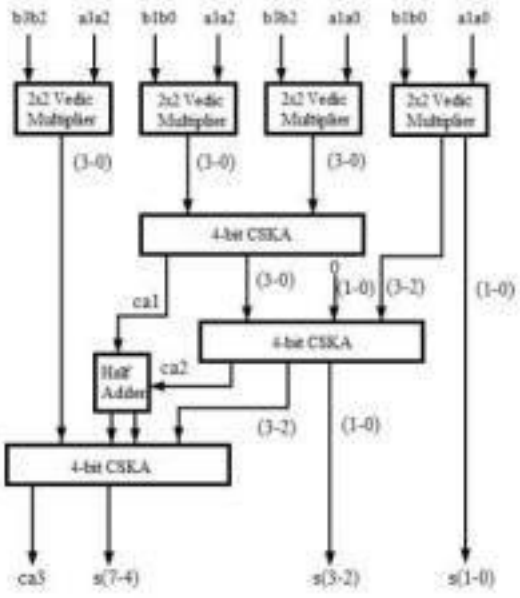


Fig.9.block diagram of 4*4 vedic multiplier

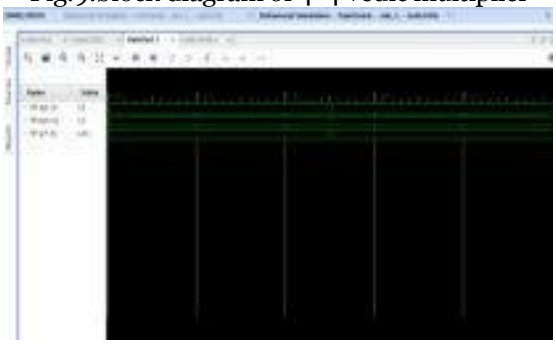

Fig.10.Output

8 bit CSA:

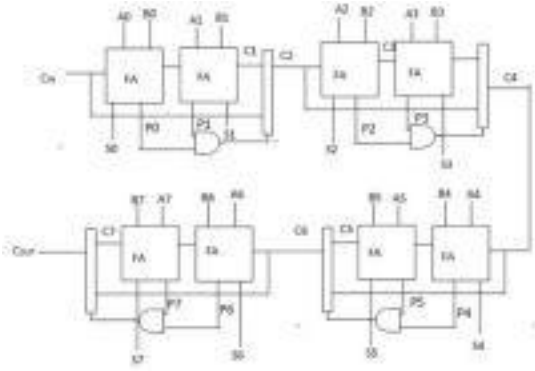

Fig.11.block diagram of 8 bit csa

Fig.12.Output

A Parallel-In-Parallel-Out (PIPO) register, alternatively called a parallel load or parallel transfer register,:
Is a digital register utilized in digital systems for storing and transferring data. Its distinctive feature

lies in its capability to load data into all of its flip-flops or storage elements simultaneously and to output all stored bits concurrently.

A D flip-flop register comprises interconnected D flip-flops arranged in parallel, facilitating the simultaneous storage and transfer of multiple bits of data. This configuration serves as a

fundamental storage unit in digital circuits and plays a crucial role in diverse applications such as data storage and serial data processing.

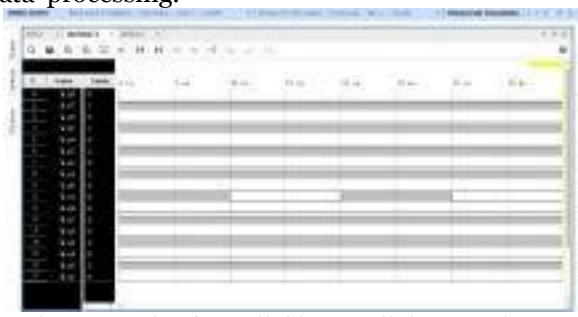

Fig:13.result of parallel in parallel out register

MAC:

Firstly The multiplier unit is tasked with executing the multiplication operation.the multiplier used in this mac is vedic multiplier,which multiplies the given 4 bit input in most effective way.in addition the adder unit is employed to perform addition operations.carry skip adder,which adds the 8 bit output of the vedic multiplier. The accumulator functions as a register or storage element responsible for storing the accumulated result. It accepts the adder's output and combines it with the current value stored in the register.the data flip flop register is used to store the result.the actual ouput will be stored in the register,and gives the final output.and again the output is given to the adder and then to accumulator,so the output changes automatically.

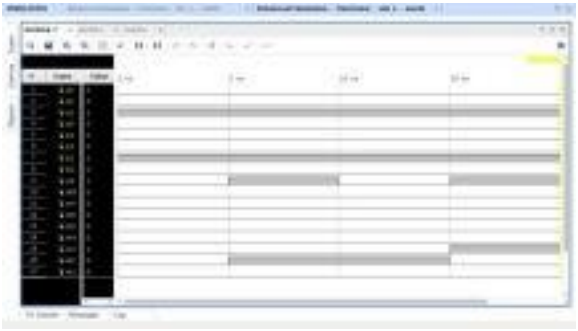

Fig.14.simulation of MAC

## CONCLUSION:

Degsined the MAC using feed forward neural network.Compared the mac output of feed forward neural network with logic gates.By utilizing dedicated ANNs in MAC block we can achieve higher computational speed and energy efficiency compared to general-purpose processors or logic gates.and also compared the vedic multiplier output of feed forward neural network with logic gates.

## RESULT:

COMPARISION TABLE:

| | TOTAL POWER | DELAY | IOB |
|---|---|---|---|
| 4 BIT VEDIC USING LOGIC GATES | 17.733W | 5.293 | 16 |
| 4 BIT VEDIC USING ANN | 17.623W | 1.770 | 17 |
| 4 BIT MAC USING LOGIC GATES | 50.161W | 34.274 | 18 |
| 4 BIT MAC USING ANN | 33.773W | 16 | 18 |

Table.1:comparision of 4 bit vedic multiplier using logic gates with ANN and comparison of MAC using logic gates with MAC using ANN

RESULT:

MAC operations benefit from the proficiency of Artificial Neural Networks (ANNs) in performing weighted summation, a fundamental operation in neural networks. The effective computation of weighted sums by ANNs can lead to optimized
power efficiency and minimized processing delays.

In table 1 describes the less power consumption and time delays in 4 bit vedic multiplier using ANN compared to 4 bit vedic multiplier using logic gates.

The table describes the less power consumption and delay in 4 bit MAC using feed forward network compared to 4 bit MAC using logic gates.

So overall using Feed forward neural networks we can achieve low power and delay

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